Yilong Zhao

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EDUCATION

2018.9 – 2021.3 **Shanghai Jiao Tong University (SJTU), Shanghai, China**
M.Eng. , Major: Computing Technology GPA: 3.49/4.0

2014.9 – 2018.6 **Shanghai Jiao Tong University (SJTU), Shanghai, China**
B.Eng. Major: Electronic Science and Technology GPA: 3.51/4.3
Minor: Business Administration

PUBLICATIONS & PATENT

- Weidong Cao, **Yilong Zhao(co-first author)**, Adith Boloor, Yinhe Han, Xuan Zhang, and Li Jiang, "Neural-PIM: Efficient Processing-In-Memory with Neural Approximation of Peripherals, " in *IEEE Transactions on Computers,* (Accepted)
- Fangxin Liu, Wenbo Zhao, Zhezhi He, Zongwu Wang, **Yilong Zhao**, Yongbiao Chen and Li Jiang , Bit-Transformer: Transforming Bit-level Sparsity into Higher Preformance in ReRAM-based Accelerator, In *Proceedings of the 40th International Conference on Computer-Aided Design (ICCAD '21).* (Accepted)
- **Yilong Zhao**, Zhezhi He, Naifeng Jing, Xiaoyao Liang, and Li Jiang. 2021. Re2PIM: A Reconfigurable ReRAM-Based PIM Design for Variable-Sized Vector-Matrix Multiplication. In *Proceedings of the 2021 on Great Lakes Symposium on VLSI (GLSVLSI '21). Association for Computing Machinery*, New York, NY, USA, 15–20. DOI:https://doi.org/10.1145/3453688.3461494
- Liu F, Zhao W, **Zhao Y**, Wang Z, Yang T, He Z, Jing N, Liang X, Jiang L. SME: ReRAM-based Sparse-Multiplication-Engine to Squeeze-Out Bit Sparsity of Neural Network. *arXiv preprint* arXiv:2103.01705. 2021 Mar 2.
- Tao Yang, Dongyue Li, Yibo Han, **Yilong Zhao**, Fangxin Liu, Xiaoyao Liang, Zhezhi He, Li Jiang, PIMGCN: A ReRAM-Based PIM Design for Graph Convolutional Network Acceleration, *ACM/IEEE Design Automation Conference, DAC*, 2021, (Accepted)
- Z. Meng, W. Oian, **Y. Zhao**, Y. Sun, R. Yang and L. Jiang, "Digital Offset for RRAM-based Neuromorphic Computing: A Novel Solution to Conquer Cycle-to-cycle Variation," *2021 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, 2021, pp. 1078-1083, doi: 10.23919/DATE51398.2021.9474179.
- Yanan Sun, Chang Ma, Zhi Li, **Yilong Zhao**, Jiachen Jiang, Weikang Qian, Rui Yang, Zhezhi He and Li Jiang, "Unary Coding and Variation-Aware Optimal Mapping Scheme for Reliable ReRAM-based Neuromorphic Computing," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 2021
- Zhuoran Song, **Yilong Zhao**, Yanan Sun, Xiaoyao Liang and Li Jiang. "ESNreram: An Energy-Efficient Sparse Neural Network Based on Resistive Random-Access Memory, "*Proceedings of the 2020 on Great Lakes Symposium on VLSI, GLSVLSI*. 2020: 291-296.
- Chaoqun Chu, Yanzhi Wang, **Yilong Zhao**, Xiaolong Ma, Shaokai Ye, Yunyan Hong, Xiaoyao Liang, Yinhe Han and Li Jiang. "PIM-Prune: Fine-Grain DCNN pruning for Crossbar-based Process-In-Memory architecture, " *ACM/IEEE Design Automation Conference, DAC*, 2020

- Jia Wang, **Yilong Zhao**, Xin Huang and Guangqiang He. "High Speed Polarization-Division Multiplexing Transmissions Based on the Nonlinear Fourier Transform, " *ZTE COMMUNICATIONS* 17, 3 (2019).
- Aiguo Sheng, **Yilong Zhao**, and Guangqiang He, "Characterization of Kerr Solitons in Microresonators with Parameter Optimization and Nonlinear Fourier Spectrum," in *Conference on Lasers and Electro-Optics, OSA Technical Digest (Optical Society of America, 2019)*, paper JW2A.47.
- Aiguo Sheng, **Yilong Zhao**, and Guangqiang He, "Quadratic soliton combs in doubly resonant half-harmonic generation," in *Nonlinear Optics (NLO), OSA Technical Digest (Optical Society of America, 2019)*, paper NTu4A.18.

Under Review/In Preparation

- **Yilong Zhao**, et. al , HPAST: A FeFET-SRAM Hybrid PIM Accelerator for Second-order Training of DNN, 2021 IEEE International Symposium on High-Performance Computer Architecture (HPCA), 2021, under review

Patent

- Li Jiang, Yilong Zhao, "Reconfigurable Architecture, Accelerator, Circuit Deployment and Dataflow Methods," Application No. 202010910280.5
- Li Jiang, Yilong Zhao, Xiaosong Cui, Yun Chen, Jianxing Liao, "Neural Network Circuit," Application No. 202010729402.0

SCIENTIFIC RESEARCH EXPERIENCE

Shanghai Qizhi Institute

A PIM based Second-Order Trainning Accelerator **Jan 2021 – now**

The purpose of the research is to design a neural network second-order optimizer based on the integration of storage and calculation technology. Including the storage and calculation integration design of some unique operators in the second-order optimization, and the design of the architecture mapping strategy.

PIM Implementation Towards Optical Communication Project **Mar 2021 – now**

The purpose of the research is to realize the receiver of optical communication and wireless communication based on the integrated technology of storage and calculation, and is responsible for the following tasks:

- Design the overall architecture of optical communication and wireless communication systems based on the integration of storage and calculation, including operator splitting and algorithm reconstruction.
- Realize the circuit simulation of some operators.
- Aiming at the high-power calculation module to achieve a lower calculation amount than the existing numerical algorithm under the conditions of allowable error.

Advanced Computer Architecture Laboratory, SJTU,

Supervisor: Prof. Li Jiang

A Reconfigurable ReRAM-based DNN Accelerator Architecture **Aug 2019 – Dec 2020**

Design a ReRAM-based DNN accelerator which can significantly reduce the peripheral circuit's overhead.

- Propose an energy-efficient ReRAM-based accelerator's peripheral circuit implement. Compare to some state-of-art architectures, the architecture improves the energy efficiency by 5.36×.
- Design a reconfigurable ReRAM-based DNN accelerator. Compare to some state-of-art architectures, the architecture improves the energy efficiency by 27×.

ReRAM-based Efficient and Reliable DNN Accelerator Project **Apr 2019 – Apr 2020**

The project investigates the enhancement of computational reliability and the utilizes sparsity to improve energy efficiency in ReRAM-based DNN accelerator. I am responsible for the following work:

- Design and code a cycle-accurate simulator for the ReRAM-based NN accelerator. The simulator is built based on GEM5.
- Rewrite the simulator to evaluate the reliability and performance of architecture for pruned NN, The results of the simulator are used as an important metric for the project evaluation.
- Design a ReRAM-based DNN accelerator for pruned NN.

Laboratory of Quantum Nonlinear Photonics (QNP), SJTU,

Supervisor: Prof. Guangqiang He

Conditions for the Generation and Evolution of Optical Frequency Combs **Mar 2018 – Jun 2018**

- Study the evolutionary conditions of optical soliton and optical frequency comb generation in optical microcavities, and build a simulation system.
- Analyze the evolution of an optical frequency comb in an optical microcavity with nonlinear eigenvalues for the first time and obtain the relationship between the number of optical solitons and nonlinear eigenvalues.

Quantum Entangled Optical Frequency Comb Generation and Transmission based on Silicon-based Micro-nano Resonant Cavity Project **June 2017 – Mar 2018**

The project investigates the use of nonlinear frequency domain coding to solve the problem of evolutionary decay of optical signals during long distance transmission. I am responsible for the following work:

- Code the nonlinear Fourier transform and its inversion modules in systems with Matlab.
- Construct the fiber optic signal transmission simulation system.

University Student Innovation Program, SJTU,

Supervisor: Prof. Chunyu Zhao

Development of DTU with Bluetooth Interface Project **Dec 2015 – Dec 2016**

Design a data transmission unit (DTU) circuit with data analysis display program. I am responsible for the following work:

- As the project leader, responsible for the progress and final reporting of the project.
- Designed and developed a DTU, including circuit design, soldering and embedded programming, and solved the problem of electromagnetic interference of the circuit in the application scenario.

TA,

Algorithm design and analysis (CS222) **SJTU, 2019-2020 Autumn**